CLAIMS

What is claimed is

1. A system for overflow and saturation processing, comprising:

an adder, operatively connected to receive first and second operands, and connected to add the operands;

an accumulator, operatively connected to store at least a portion of the added operands or at least a portion of a selected one of predetermined constants based on control signals;

guard bits, operatively connected to store the remaining portion of the added operands or the remaining portion of the selected one of predetermined constants based on the control signals;

overflow logic operatively connected to the accumulator and to the guard bits so as to indicate overflow of the accumulator; and

saturation logic, operatively connected to the adder, to the guard bits, and connected to provide the control signals based on at least a portion of the added operands at least a portion of the guard bits.

2. The system according to claim 1, wherein the saturation logic includes:

logic means for comparing most significant bits of the guard bits and most significant bits of the added operands, and for generating the control signals in accordance with the comparison.

3. The system according to claim 2, wherein the saturation logic includes:

a selector operatively connected to selectively provide one of the added operands or one of the predetermined constants based on the comparison.

4. The system according to claim 2 , wherein the logic means includes:

means for providing the control signals in accordance with an enable signal and in accordance with the comparison.

5. The system according to claim 4, wherein the logic means further includes:

means, responsive to the comparison, for selectively providing the control signals so that the accumulator stores at least a portion of the added operands and the guard bits store the remaining portion of the added operands, or the accumulator stores at least a portion of a predetermined constant and the guard bits store the remaining portion of the predetermined constant.

6. A method for overflow and saturation processing in a processor including guard bits and an accumulator, comprising:

adding operands to form a result;

comparing a portion of the result with a portion of the guard bits;

storing either a portion of the result in the accumulator and the remaining portion of the result in the guard bits, or a portion of a selected predetermined constant in the accumulator and the remaining portion of the predetermined constant in the guard bits in accordance with an enable signal and the result of the comparison.

7. The method according to claim 6, wherein the comparing a portion of the result with a portion of the guard bits includes comparing most significant bits of the guard bits and most significant bits of the result.